

Birla Institute of Technology and Science, Pilani- KK Birla Goa Campus II Semester 2015-2016

EEE/CS/INSTR F241/ Microprocessor Programming and Interfacing

Time	: 60 min.	omprehensive Examination- Part A (O Date: 6-5-2016	pen Book) MM: 30
(Not	e: Answer Part A on the	Q-Paper itself and Part B on a so	eparate answer sheet provided.)
ID	No.:	Name:	Section
<u>Q1.</u>	Give two possible opcodes	s for the following instruction runni	ing on 8086: MOV AX, [2345 _H]
	A1 45 23		
	8B 06 45 23		[3]
<u>Q2.</u>	V _{REF} + of ADC 0808 is conne difference that can be det		ed to 0V. What will the minimum voltage [2]
	15.625mV		
<u>Q3.</u>	•	$_{0}$ 8255 is connected to data lines D_{0} ort A, Port B, Port C and the contro	$_{0}$ -D ₇ . The starting address of 8255 is 30 _H . If Register? [2]
	Port A- 30 _H , Port B – 34	н, Port C – 38н , Control Register	r — 3C _H
<u>Q4</u> .	How many 8259's are req	uired for 64 Interrupt Inputs?	[2]
	9		
<u>Q5.</u>	What is the maximum am	ount of memory required for storin	ng the GDT? [1]
	64k		

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	<u>Q6.</u>	Q6. The descriptor of an 80286 Processor stored in the GDT is as follows 00 00 B1 32 00 00 3F MSB onwards] Answer the following questions with respect to this descriptor [1+1+1+1+1+1+1+1+1+1+1+1+1+1+1+1+1+1+1+								[From				
		(i)	Staring address of the Segment is 32 00 00 _H											
		(ii)	Size of	the seg	ment is		16K							
		(iii)	The mi	inimum	CPL and	RPL re	quired to	o acces	s this se	egment	01			
		(iv)	Is the s	segmen	t code or	data s	egmentî	?	Dat	a				
	<u>Q7.</u>		ata 0011 Ita. Assui						ıs. Draw	v the NF	ZI encod	ded data	pattern [4]	for
V _														
	<u>Q8.</u>	Write ar	JNC	X1	uage pro	gram se	egment [:]	to do tł	ne follov	wing fur	nction: J	C 3FFH	[3]	
		X1:	JMP	3FF _H										
	Q9. If INTR is raised during a DIV instruction execution and the DIV instruction results in a divide interrupt – what will be the order in which the interrupts are serviced? [1]									n a divid [1]	e by 0			
		INTO 1	followe	d by IN	TR									
	<u>Q10.</u>	If the DF	PL of a ca m CPL an	_							_			ıld the
		10		0						.,		<u> </u>	-1	

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Q11. Which type of cache miss is reduced in set associative caches when compared to direct-mapped caches? [1]

Conflict Miss

Q12. If the cache access time is 5ns, the access of main memory is 25ns and we require an average memory access time of 10ns. What should be the hit rate of the cache? [assuming that there is only one level of cache in the system.]

75%

Q13. Write a sub-routine that can be used for transferring data from HDD to memory location using DMAC 8237. The starting address of the DMAC is 80H. The HDD uses burst transfer of up to 1K of data/burst. The starting address of memory location to which the transfer must be done is 06000H. DMA channel 0 is used by HDD- HDD DREQ is active high, DACK is active low. [3]

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СН0	EQU	80H
CH0C	EQU	82H
MR	EQU	96H
CR	EQU	90H
MASKS	EQU	9EH
CFF	EQU	98H
	MOV	AL,01
	OUT	CFF,AL
	MOV	AL,00
	OUT	CH0,AL
	MOV	AL,60H
	OUT	CH0,AL
	MOV	AL,0FFH
	OUT	CH0C,AL
	MOV	AL,03H
	OUT	CH0C,AL
	MOV	AL,10000100B
	OUT	MR,AL
	MOV	AL,0EH
	OUT	MASKS,AL
	MOV	AL,0000 0000B
	OUT	CR,AL

Recheck Request			

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