CS/ECE/EEE/INSTR F241 – MICROPROCESSOR PROGRAMMING & INTERFACING

MODULE 1: INRODUCTION TO MICROPROCESSORS

QUESTIONS

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Binary Arithmetic

Q1. What will be the result and what will be the nature of the result in terms (All operations should be done using sign- magnitude form of representation)

- is the result zero
- is there a carry
- is there an auxiliary carry
- is the result negative
- is there an two's complement overflow
- Is the result even or odd parity

(a) 44 + 52
(b) 97 + 48
(c) 99 - 33
(d) 33 - 99
(e) -29 + -32
(f) -41 - 95
(g) 100 + 28
(h) 27 – 100

Q2. Is there a possibility of two's complement overflow during subtraction?

Q3. Perform the following operations using Booth & Modified Booth.

(a) 4 x -3
(b) -2 x -3
(c) -7 X 2
(d) 7 x 6

If addition takes 2 clock cycle and shift takes 1 clock cycle and if the clock frequency is 5 MHz, what will be the time taken to execute the above operations ?

CPU

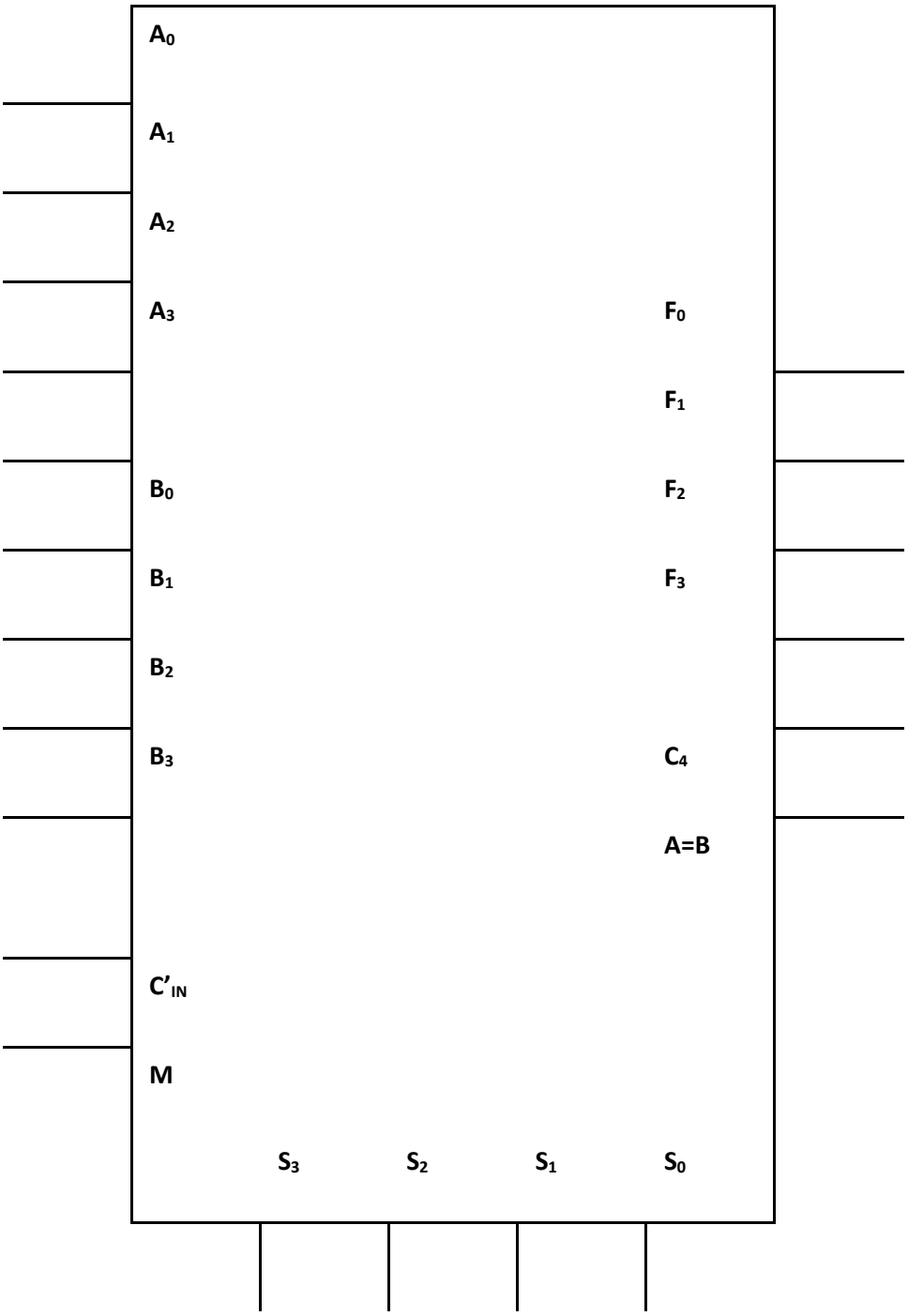
Q4. Distinguish between ISA, Micro-architecture and Physical Implementation.

Q5. How do you determine whether if a microprocessor is 8 bits or 16-bits or 32-bits?

Q6. What is the order in which the microprocessors buses (Address, Data and Control) are activated?

Q7. Three, 16 bit numbers are stored in memory location 'a',' b' and 'c'. Write ALP programs for adding the 3 numbers for CISC and a RISC processor. Assume that CISC processor has two temporary storage registers and RISC processor has 8 registers. The result is to be stored in memory location 'd'. The instructions involving ALU follow 3 operand format .Compare the performance of the CISC & RISC Processor.

Q8. Given the following ALU chip (ALU 181)



- $S_3 – S_0$
  - Selects ALU operation to perform
- M
  - 1–Logical
  - 0-Arthimetic
- C_{IN}
- C_4 along with A= B can be used for unsigned comparison

(a) What will be the size of CPU built around this ALU

(b) If other than ALU operations- the processor performs

- Load data from mem to reg
- Store dats from reg to mem
- Move data from reg to reg
- 1 Unconditional Branch
- 4 Conditional branches
- 1 Call
- 1 Return

And Instruction is of the format – Opcode dst,src , All ALU operations are performed on registers, There are totally 16 Registers R_0- R_{15} .

(c) What type of Architecture does the processor implement?
(d) What will be the normal size of the instruction?
(e) If the Processor can support 64KB of memory and Memory is byte organised- How many address are required?
(f) What will the number by which the Program Counter be incremented to support the normal sized instruction?
(g) Can you think of any other major digital modules that the processor may require?