Birla Institute of Technology & Science, Pilani

Microprocessor Programming & Interfacing - Answer Book Part B

Only Answer in space provided

Name: _____ ID No: _____

Question No	Marks	Question No.	Marks
Q1a		Q1d	
Q1b		Q1e	
Q1c		Q1f	
Total			

Recheck Request:

5-6-2016

Q1 a

Memory Address Mapping

ROM1 – 00000H 0FFFFH

ROM2 – 10000H 1FFFFH

ROM3 – 20000H 2FFFFH.

ROM4 – 30000H 3FFFFH.

ROM5 – 40000H 4FFFFH

RAM1 – 50000H 5FFFFH

* all addresses.

RAM2 60000 – 6FFFFH

RAM3 70000 – 7FFFFH.

RAM4 80000 – 8FFFFH

RAM5 90000 – 9FFFFH

RAM6 A0000 – AFFFFH.

ROM6 B0000 – BFFFFH

ROM7 C0000 – CFFFFH.

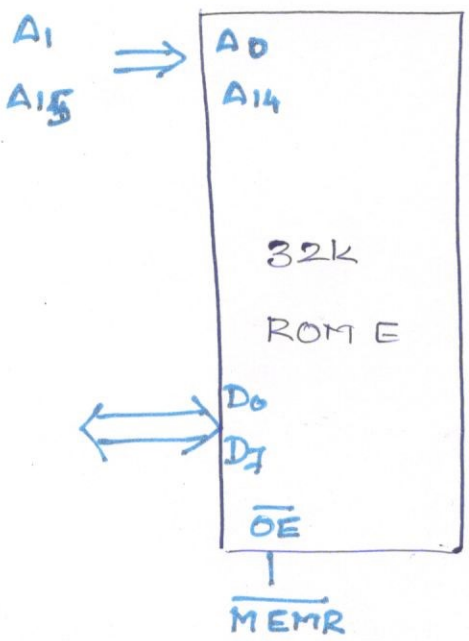
ROM8 D0000 – DFFFFH.

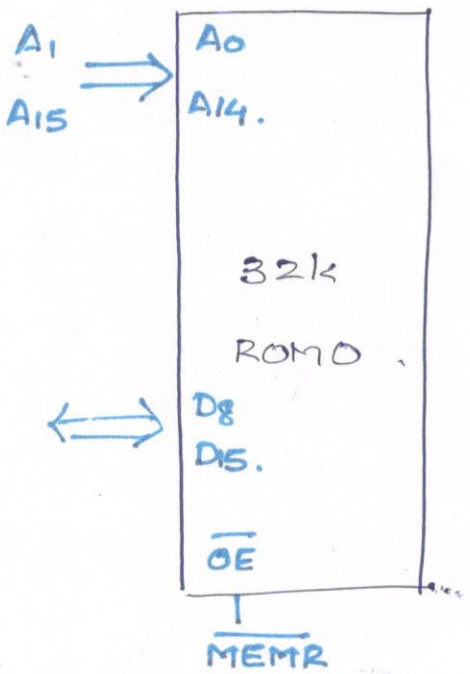
ROM9 E0000 – EFFFFH

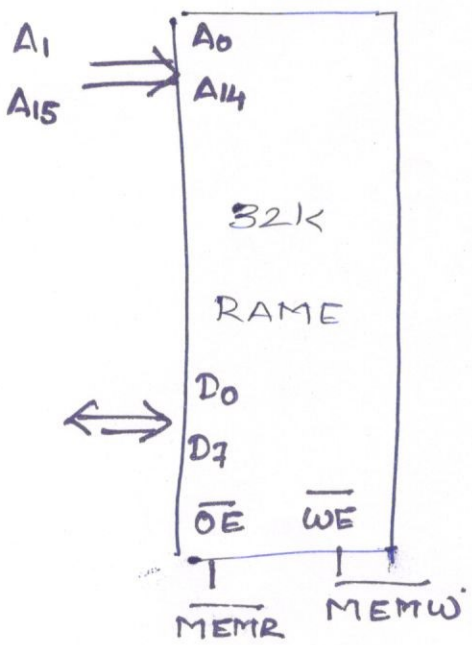
ROM10 F0000 – FFFFFH

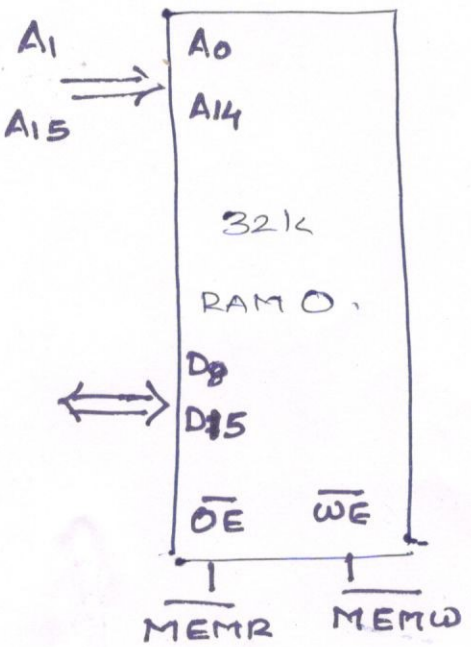
[6]

Memory Decoding









Address + Data — 2M

Control Signal — 1M

Q1b

I/O Address Mapping

8255 20 – 26H

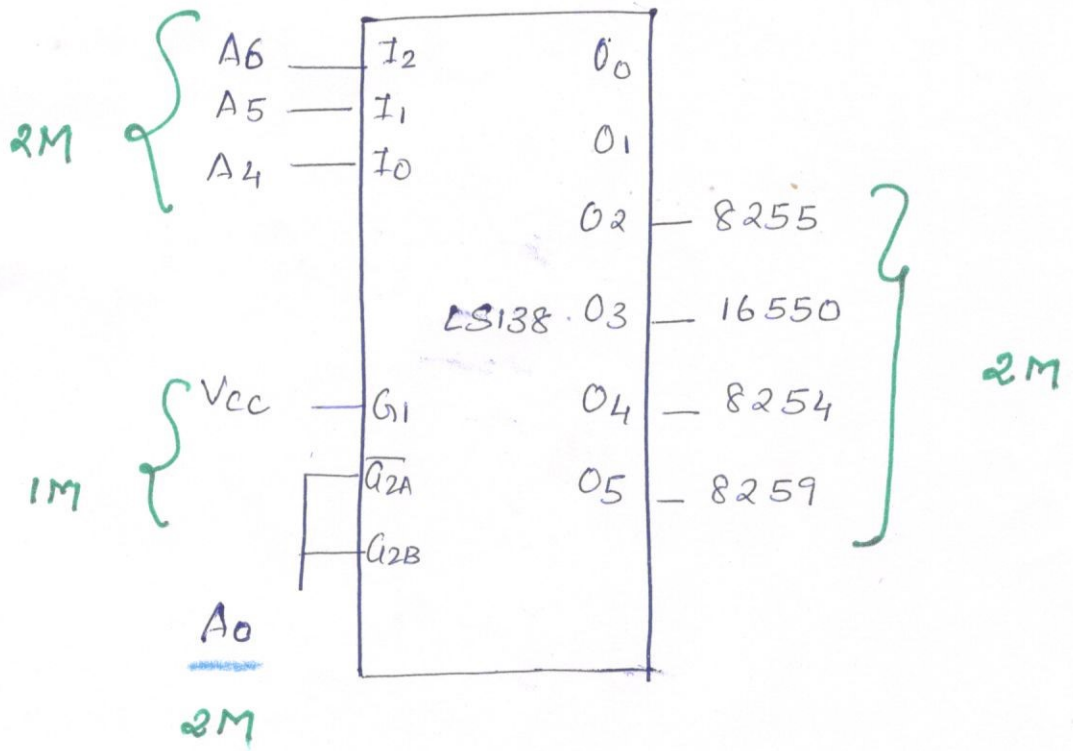
8254 40 – 46H

16550 30 – 3EH

8259 50 – 52H

[3M].

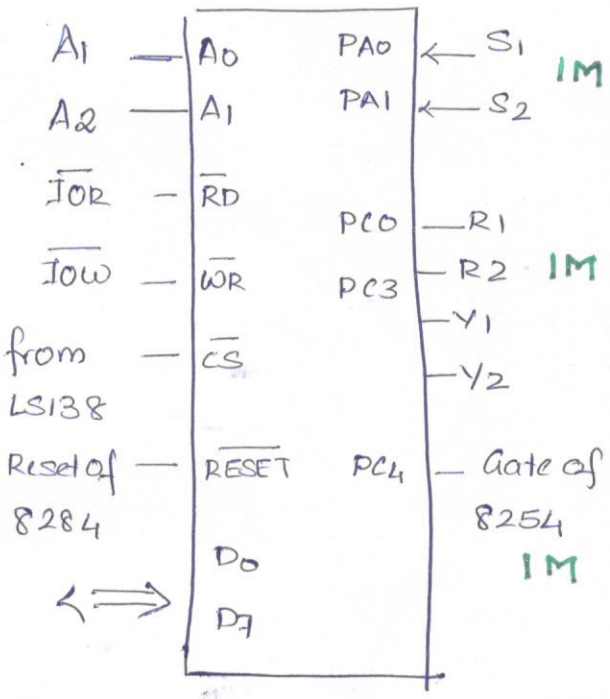
I/O Decoding



Q1 C

8255 Interfacing

1M



8255 Initialization

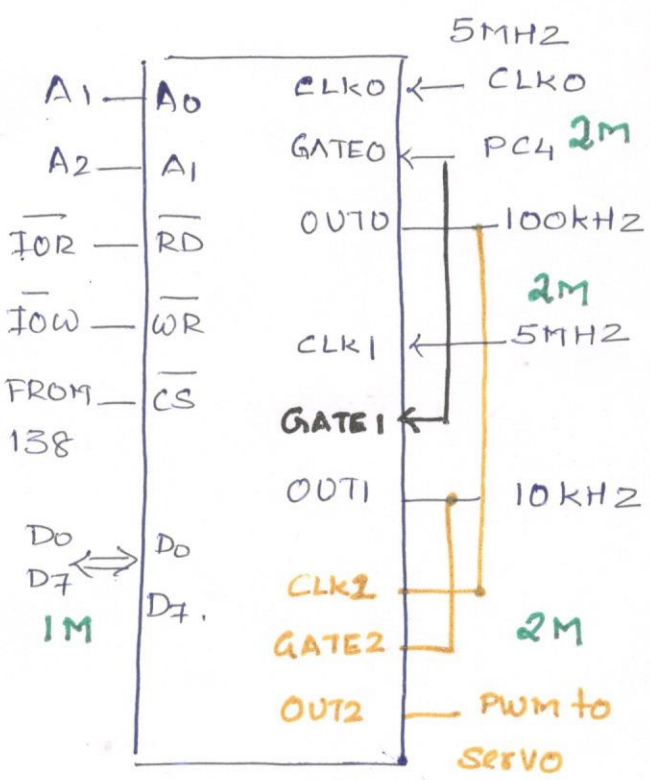
mov al, 10010010_B.

out 26h, al

1M

Q1d

8254 Interfacing



8254 Initialization

```
mov al, 00110100
out 46h, al          1M

mov al, 01110100
out 46h, al          1M

mov al, 10110010
out 46h, al.         1M.
```

8254 Count of Timers for 10KHz PWM at 20% ~~60%~~

Timer 0 – 50

Timer 1 – 500

Timer 2 – 08

2M

8254 Count of Timers for 10KHz PWM at 60%.

Timer 0 – 50

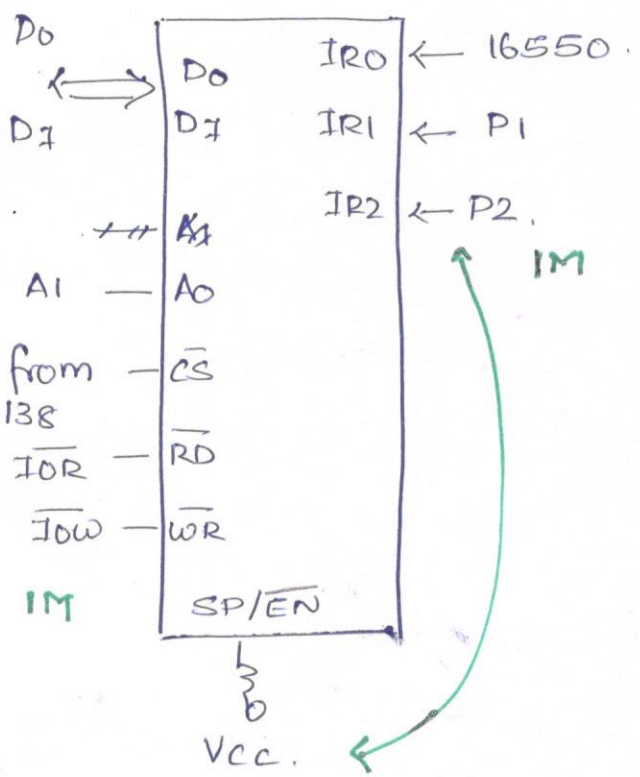
Timer 1 – 500

Timer 2 – 04

2M

Q1e

8259 Interfacing



8259 Initialization

mov al, 00010011$_B$

out 50h, al 2M

mov al, 60h

out 52h, al 1M

mov al, 00000011$_B$

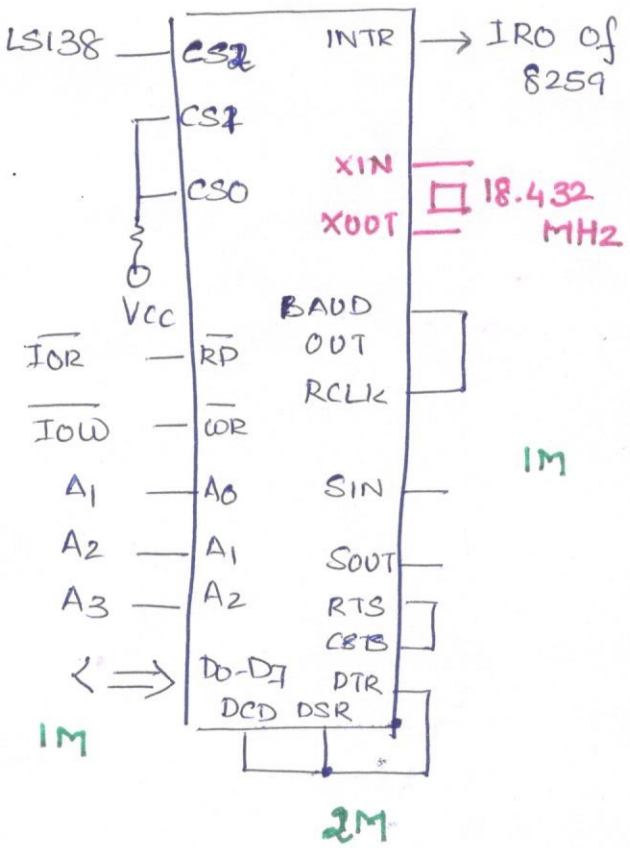
out 52h, al 2M

mov al, 1111 1000$_B$.

out 52h, al. 1M

Q1f

16550 Interfacing



16550 Initialization

```
mov al, 10001011B
out 36h,al.        1M
mov al, 60.
out 30h,al
                   2M
mov al,00
out 32h,al
mov al, 00010111B.
out 36h,al
mov al, 01000011B.
out 34h,al.        1M
```