Birla Institute of Technology & Science, Pilani- KK Birla Goa Campus							
II Semester 2015-2016							
EEE/CS/INSTR F241- MICROPROCESSOR PROGRAMMING AND INTERFACING							
Quiz 6 (Open Book)							
Date: 29-04-2016	Max Marks: 10	Duration: 30 Mins					
ID No.	Name:						

Q1. There is only a single cache in processor based system and the cache access time is 10ns with a hit rate of 85%. The main memory access time is 25ns what is the average memory access time? (4)

## 0.85x 10ns + 0.15x 25ns = 12.25ns

Q2. The table below shows the threads with their priorities in a multi-threading system. The threads which will complete in one-time slot are shown by columns that are shaded.(6)

Fill in the threads that will be executed in timeslots 1 -12 – assuming that no new threads are available for execution

THREAD	TH1	TH2	TH3	TH4	TH5	TH6	TH7	TH8
Priority	1	7	3	4	6	2	8	5

Fill in the threads that will be executed in timeslots 1 -12 – assuming that no new threads are available for execution

Time slot	1	2	3	4	5	6	7	8
Thread	TH1	TH6	ТН3	TH4	TH8	TH5	TH2	TH7
Time Slot	9	10	11	12				
Thread	TH6	TH3	TH2	TH7				