Q1

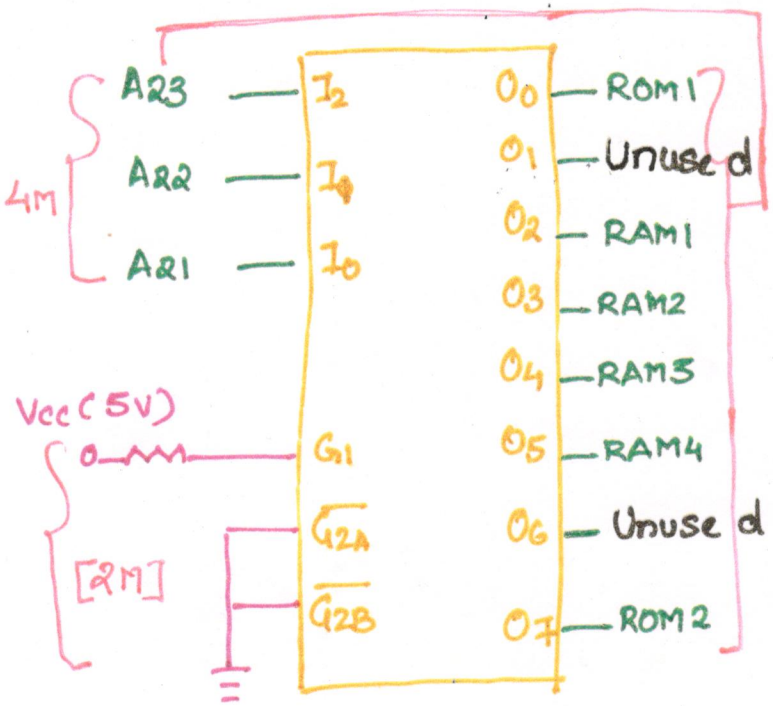
Memory map

ROM1 :	00 00 00H	1F FF FFH
ROM2 :	E0 00 00H	FF FF FFH
RAM1 :	40 00 00H	5F FF FFH
RAM2 :	60 00 00H	7F FF FFH
RAM8 :	80 00 00H	9F FF FFH
RAM4 :	A0 00 00H	BF FF FFH.

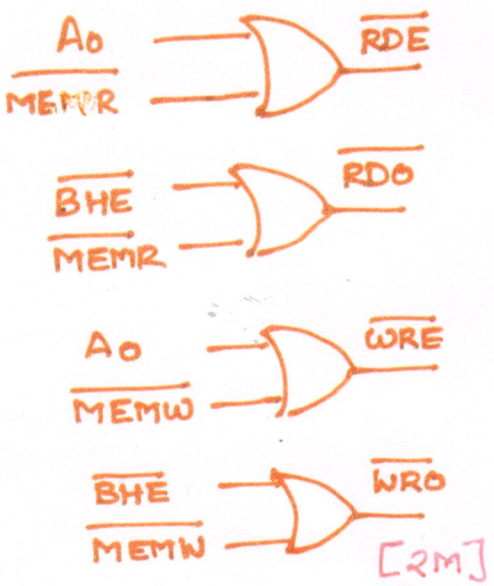
[2M]

[6M]

Memory Decoding

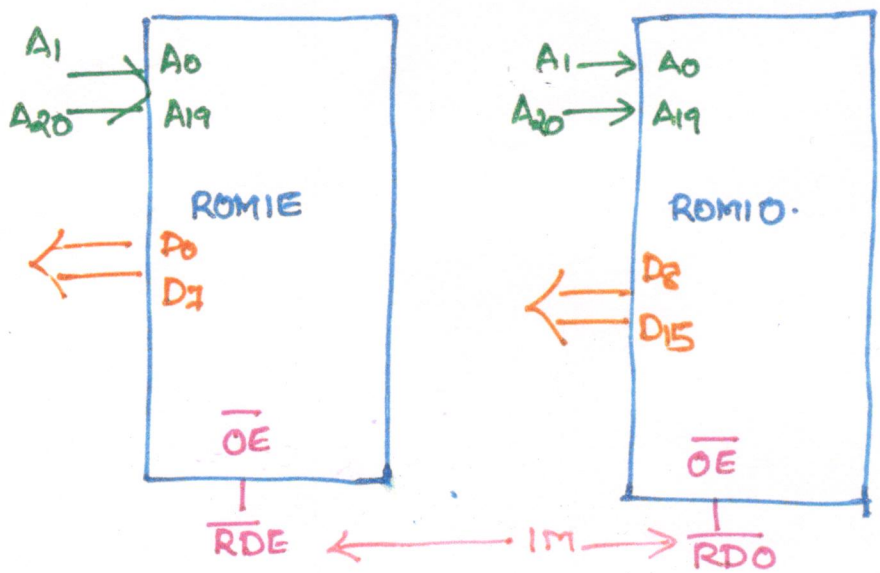


Memory Bank



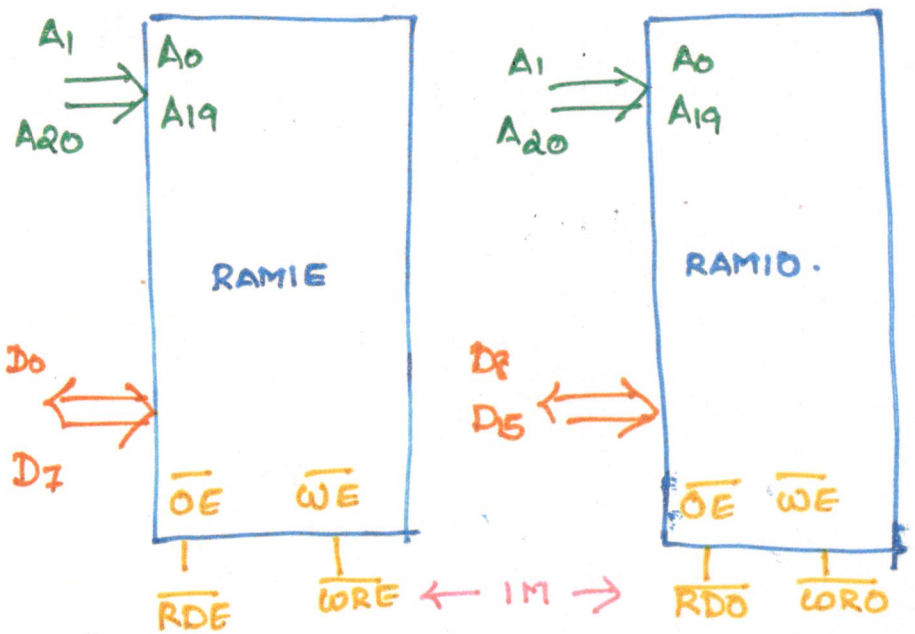
[2M]

Memory Interfacing

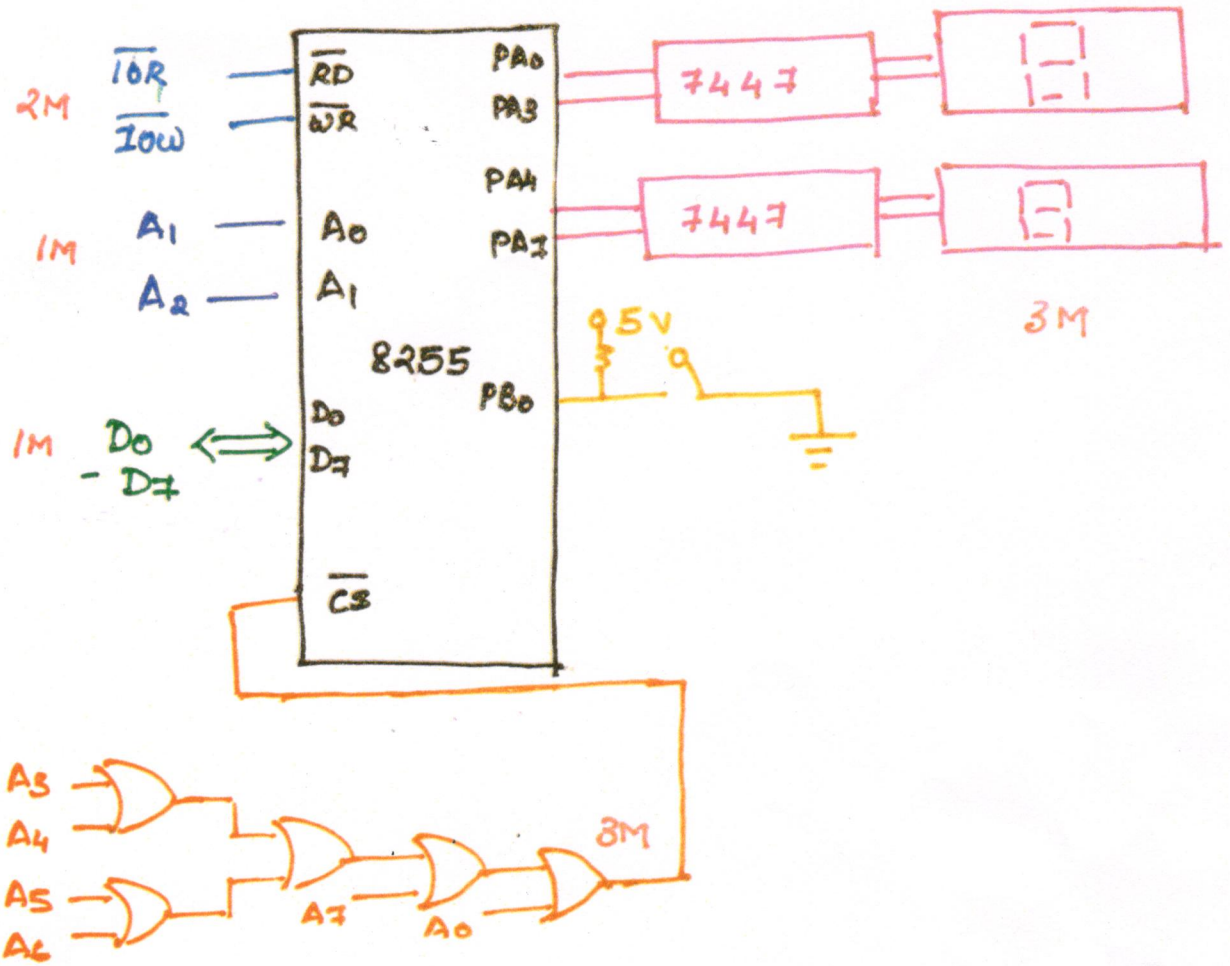


1M - Address all chips

1M - Data all chips



Q2



ALP

```
mov  al, 88h        2M
out  06h, al

mov  al, 00h
out  00, al         1M

x1:  in   al, 02h   1M
     and  al, 01h   1M
     jz   x1
```

```
     mov  cx, 99
     mov  al, 01h
x2:  out  00h, al   4M
     add  al, 01
     daa

     call d_hs      1M
     loop x2
```