



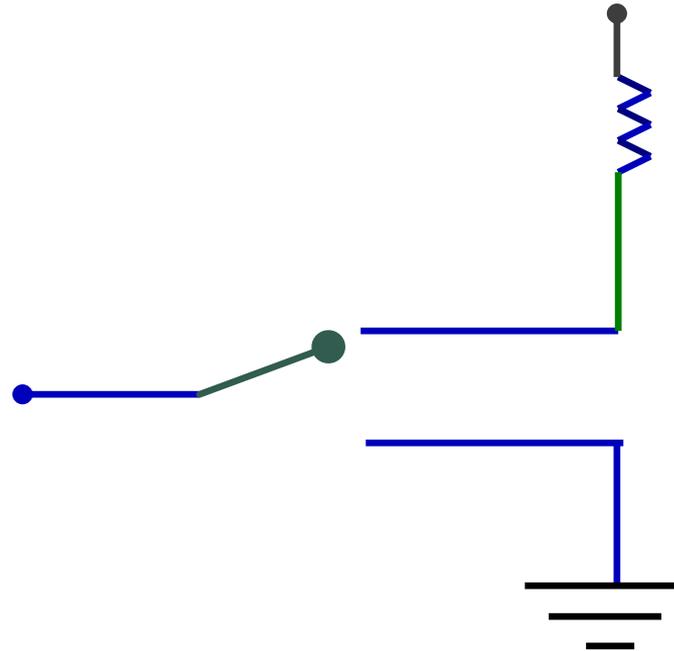
PROTEUS SYSTEM DESIGN EXAMPLE





A 8086 based system checks a set of 8 switches (SW1- SW8) every 1 second and displays the no. of switch that is closed(assume only 1 switch is closed at a time) - if no switch is closed - 0 is displayed.

SWITCH – SINGLE POLE DOUBLE THROW SWITCH

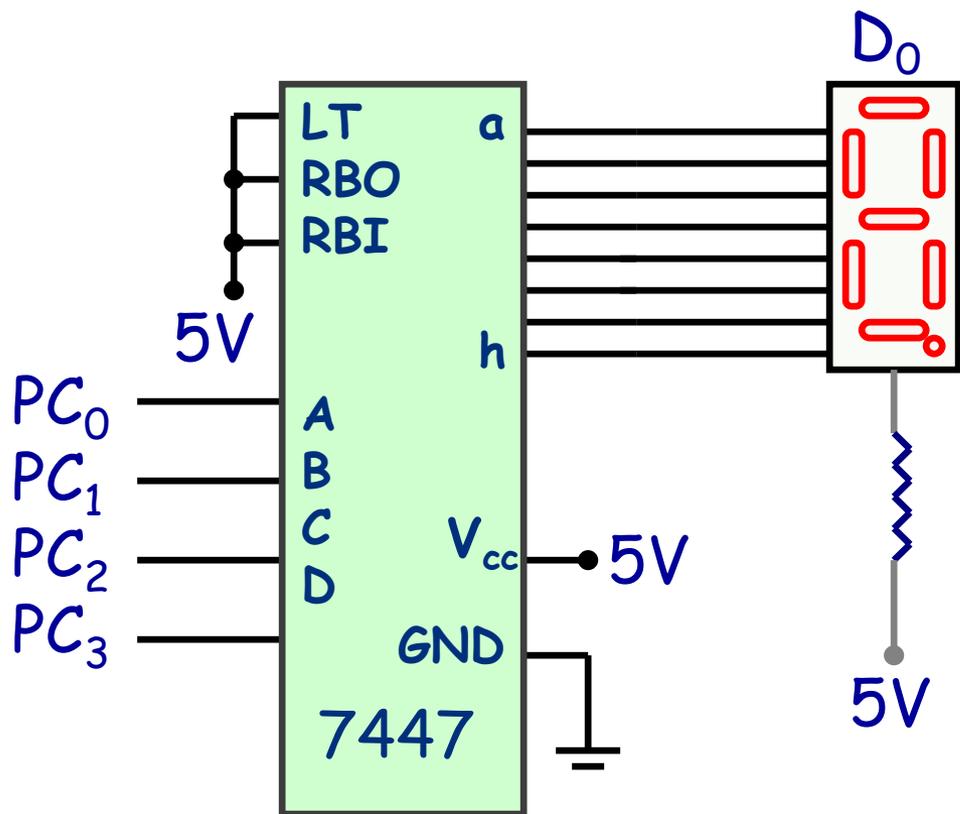


INTERFACE TO SWITCH

- 8 switches
- $PB_0 - PB_7$ (SW1 - SW8)

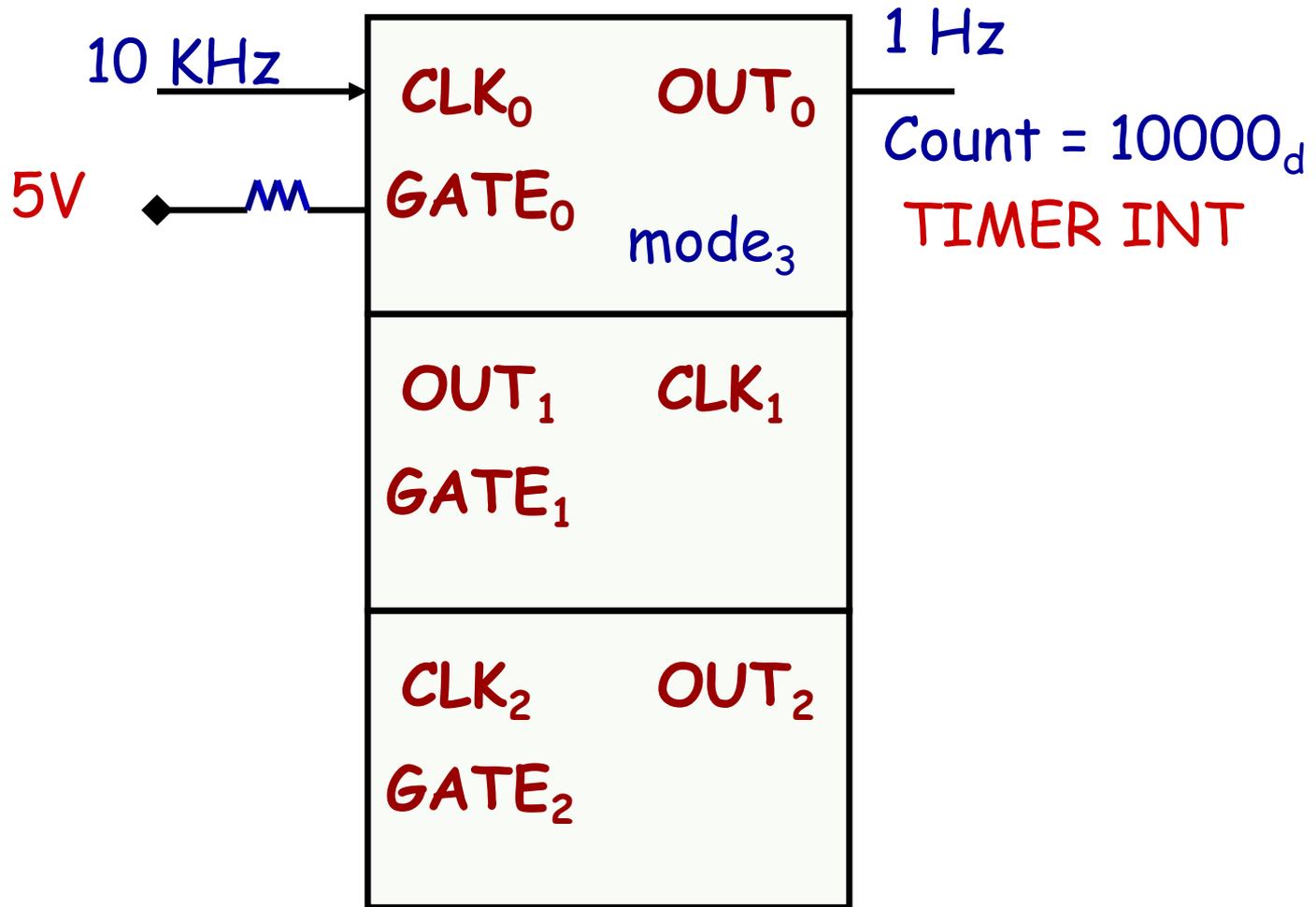
7 SEGMENT DISPLAY

- I – seven segment displays
- I- 7447
- Requires 4-bit



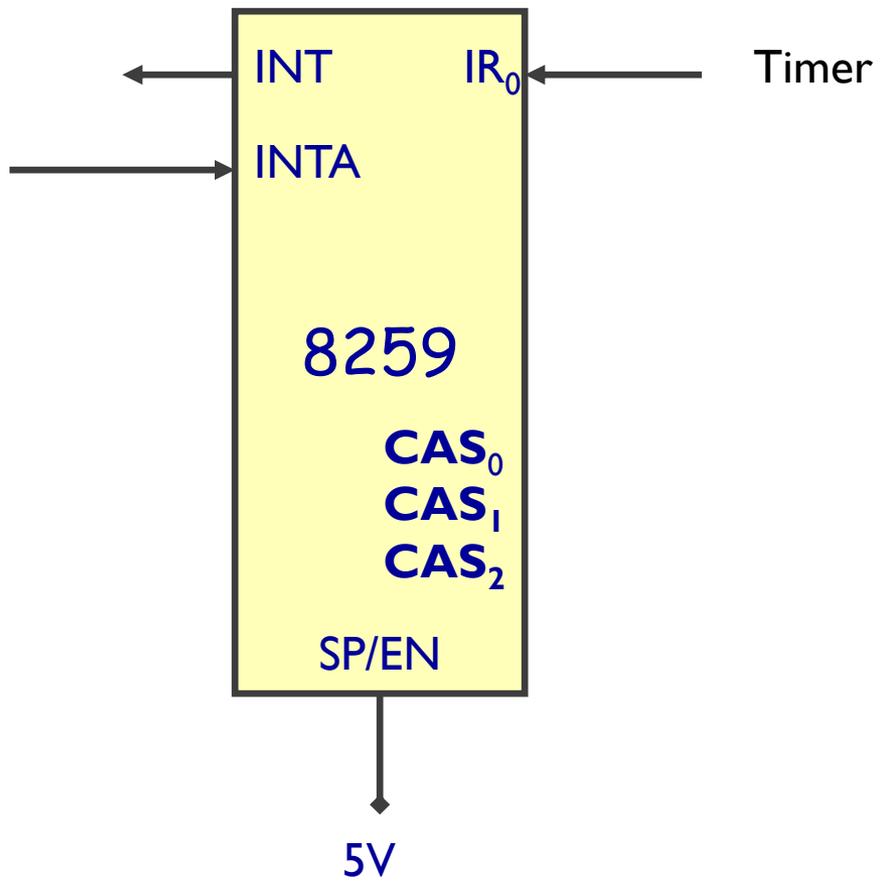
I SEC INTERRUPT

- Use 8253 as only that is available in proteus
- Clock has to be generated using pulse generator using 10KHz – if a higher frequency is used – pulse will not be proper- as rise and fall time of pulse in proteus can be set to a minimum of $1\mu\text{s}$ – and the rise and fall time are should be less than 1 % of frequency.



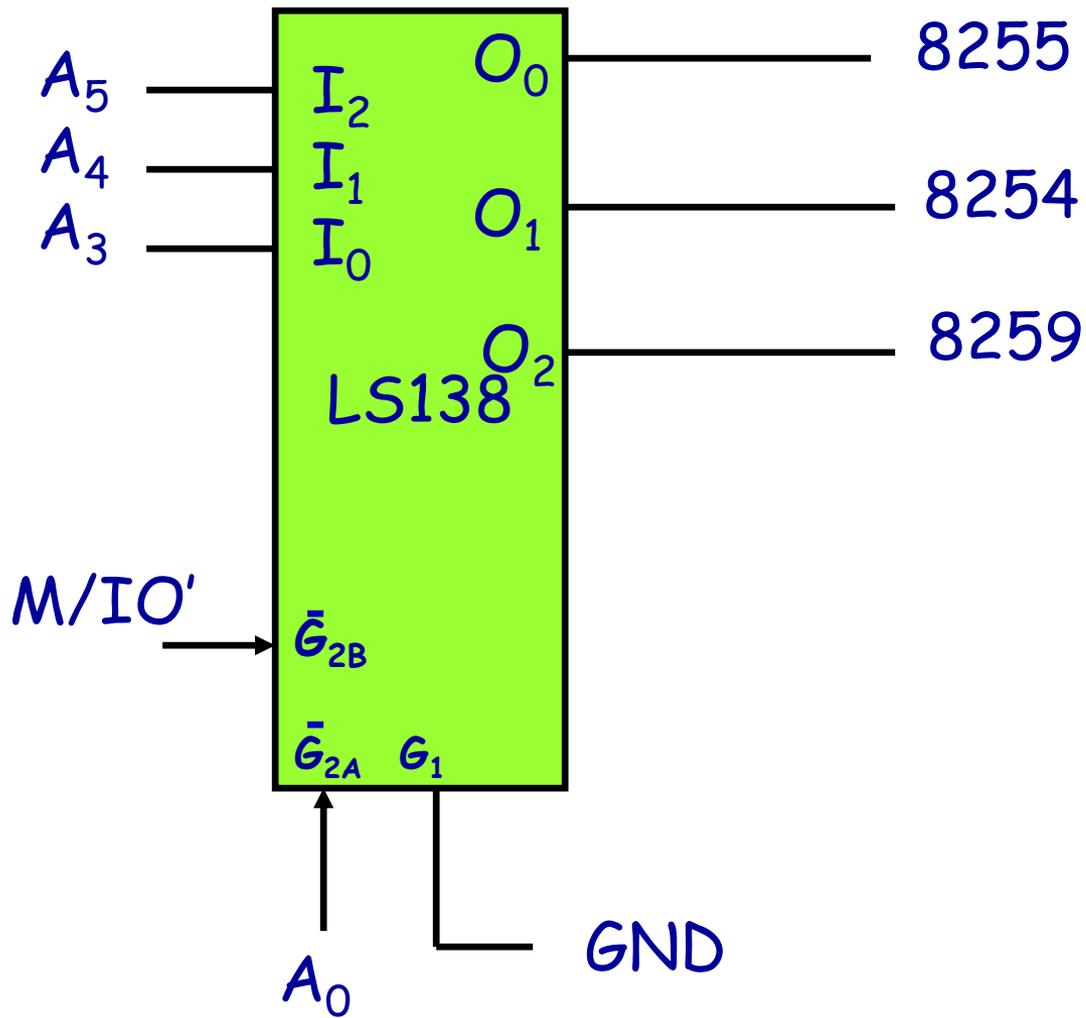
INTERRUPT GENERATION

- Use 8259



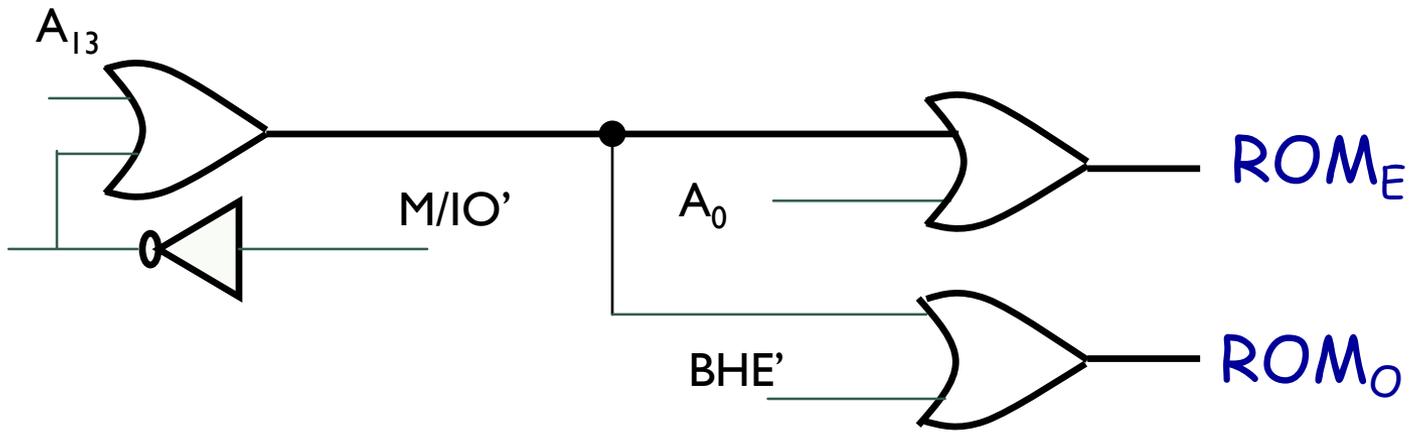
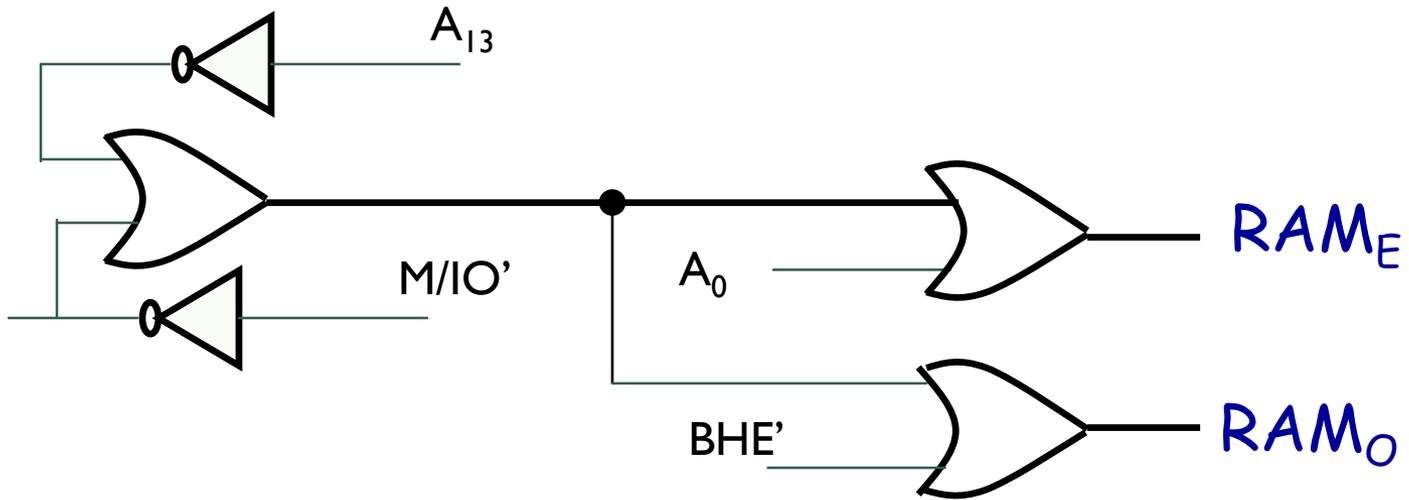
INTERFACE 8255, 8254 & 8259

- Fixed addressing
- Address
- $00 - 06_{\text{H}}$ - 8255
- $08_{\text{H}} - 0E_{\text{H}}$ - 8254
- $10_{\text{H}} - 12_{\text{H}}$ - 8259
- Incremental Addressing

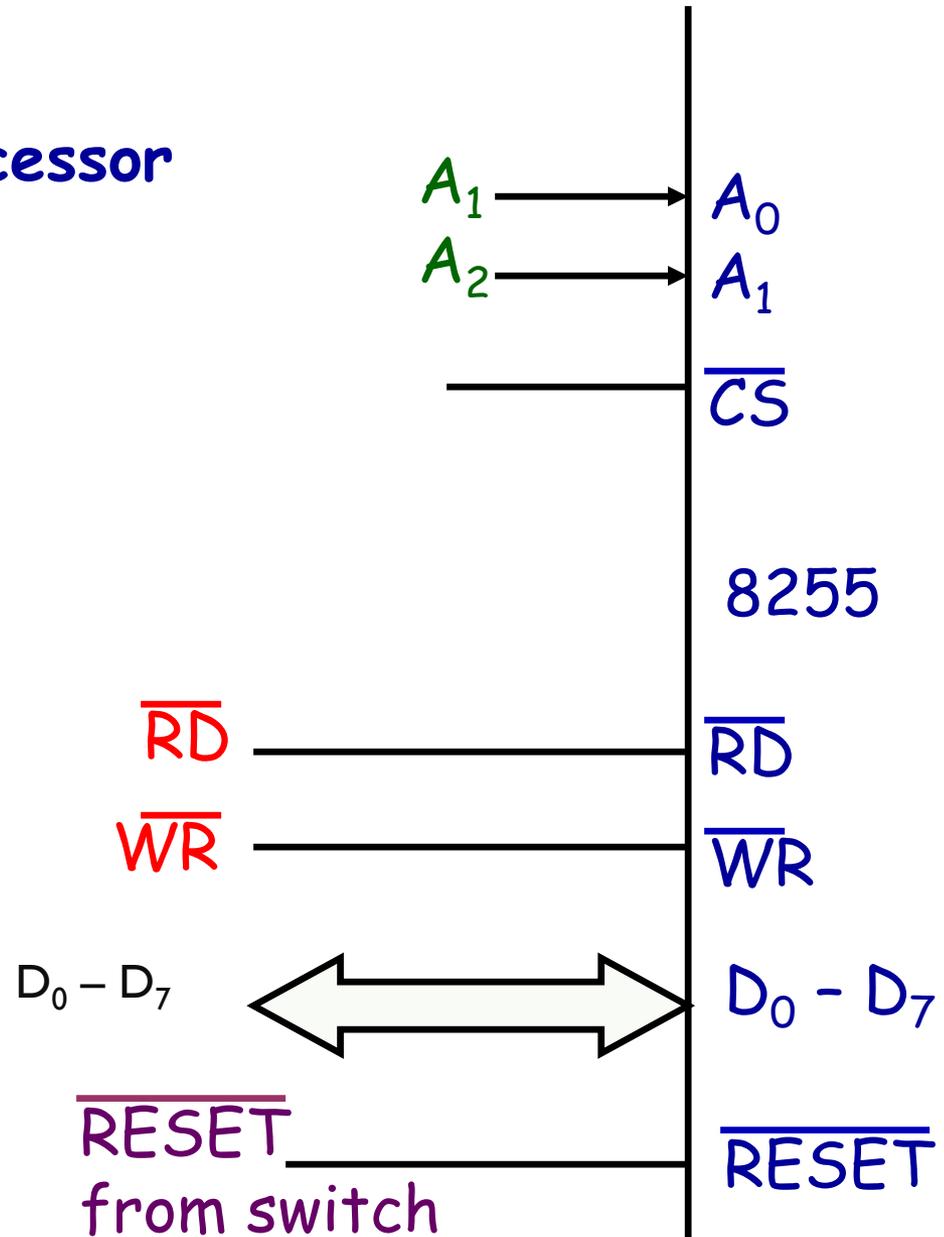


INTERFACE MEMORY

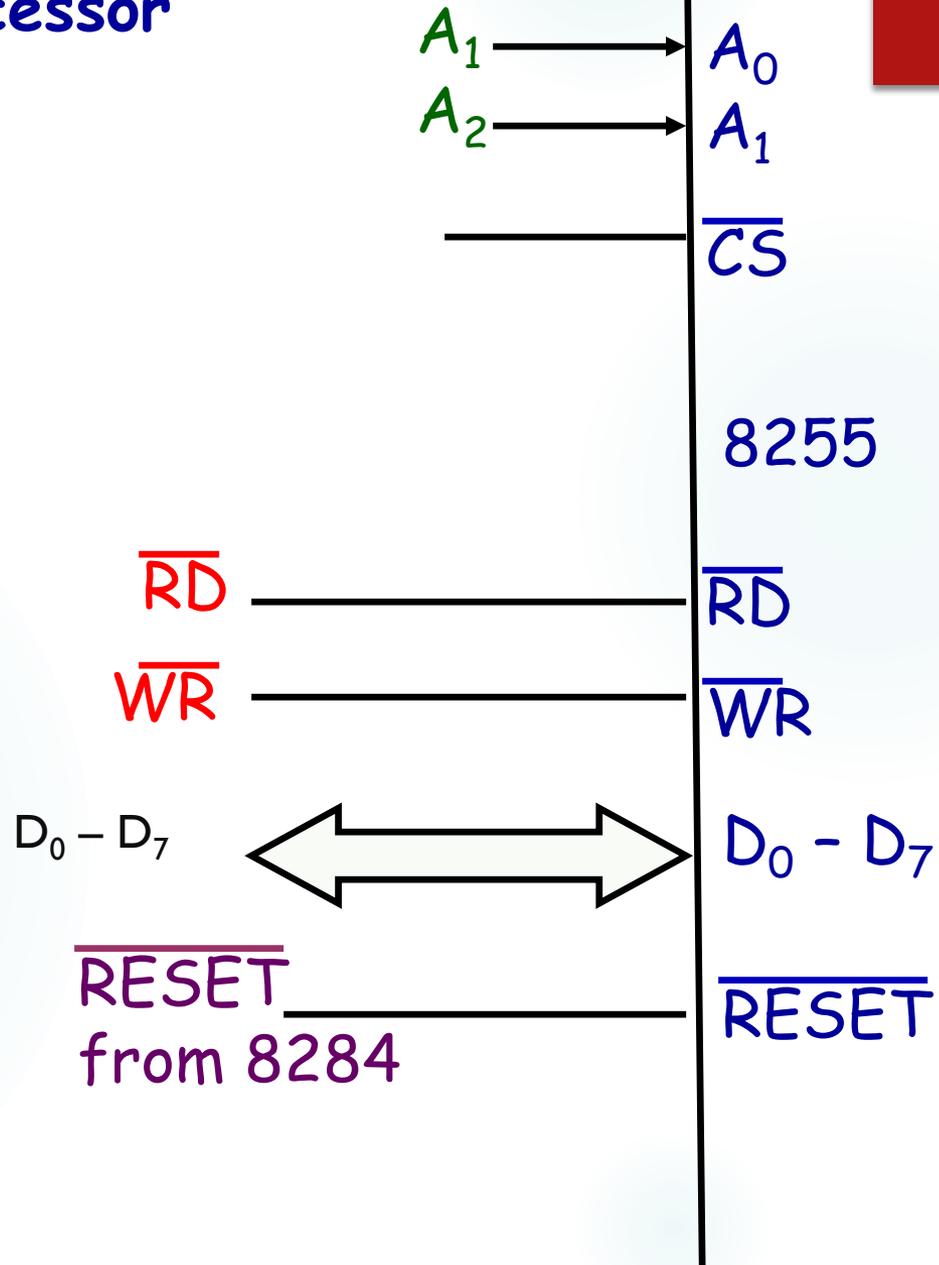
- RAM – minimum 2k chip- 4k
- ROM – in proteus 7 is minimum 4k chip – 8k
- ROMI 00000_H - $01FFF_H$
 - This is ok as proteus allows you to set reset address I have set it to 0000:0400(CS:IP)
 - This the area after IVT
- RAM 02000_H – $02FFF_H$

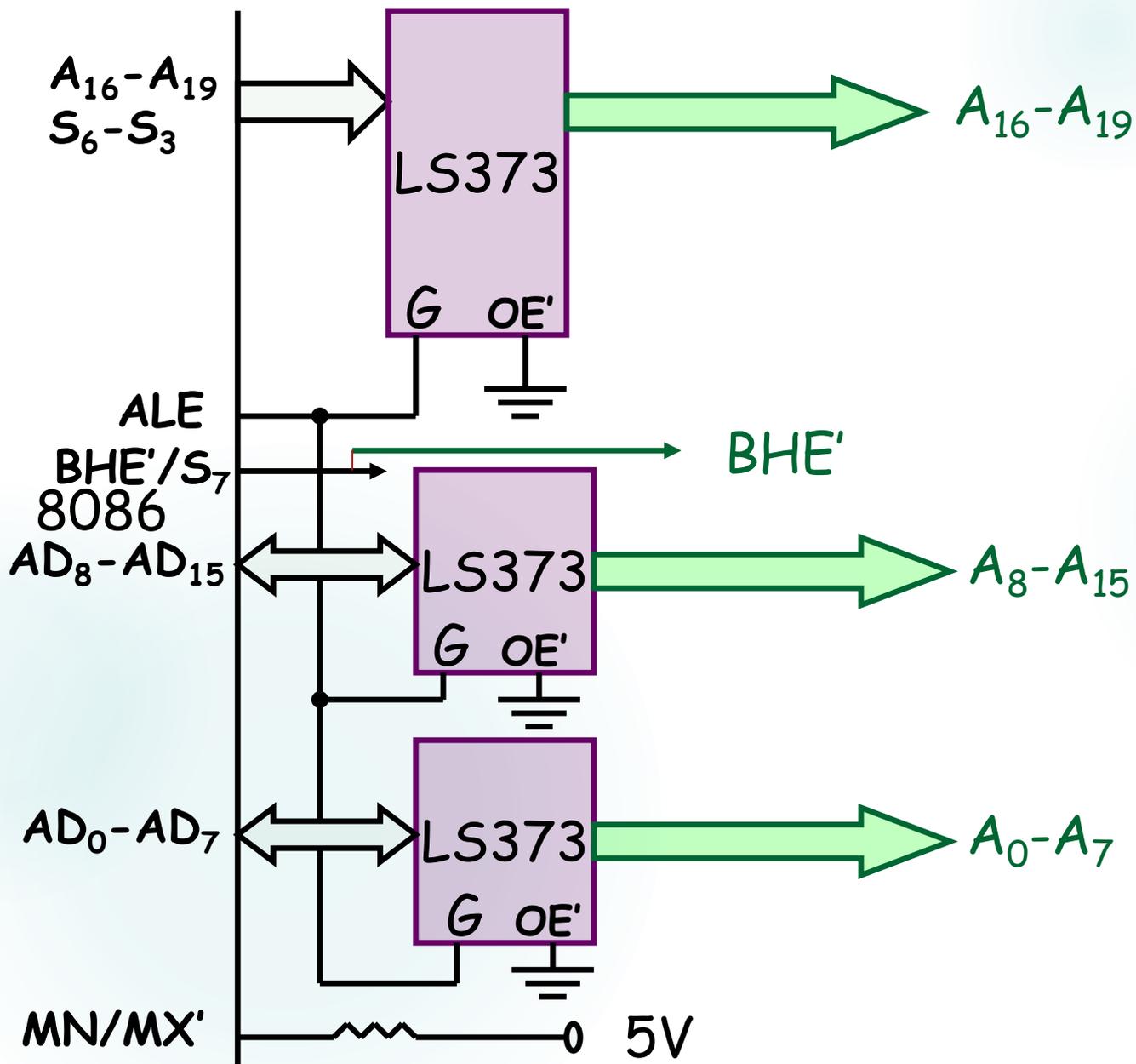


Interface to the processor

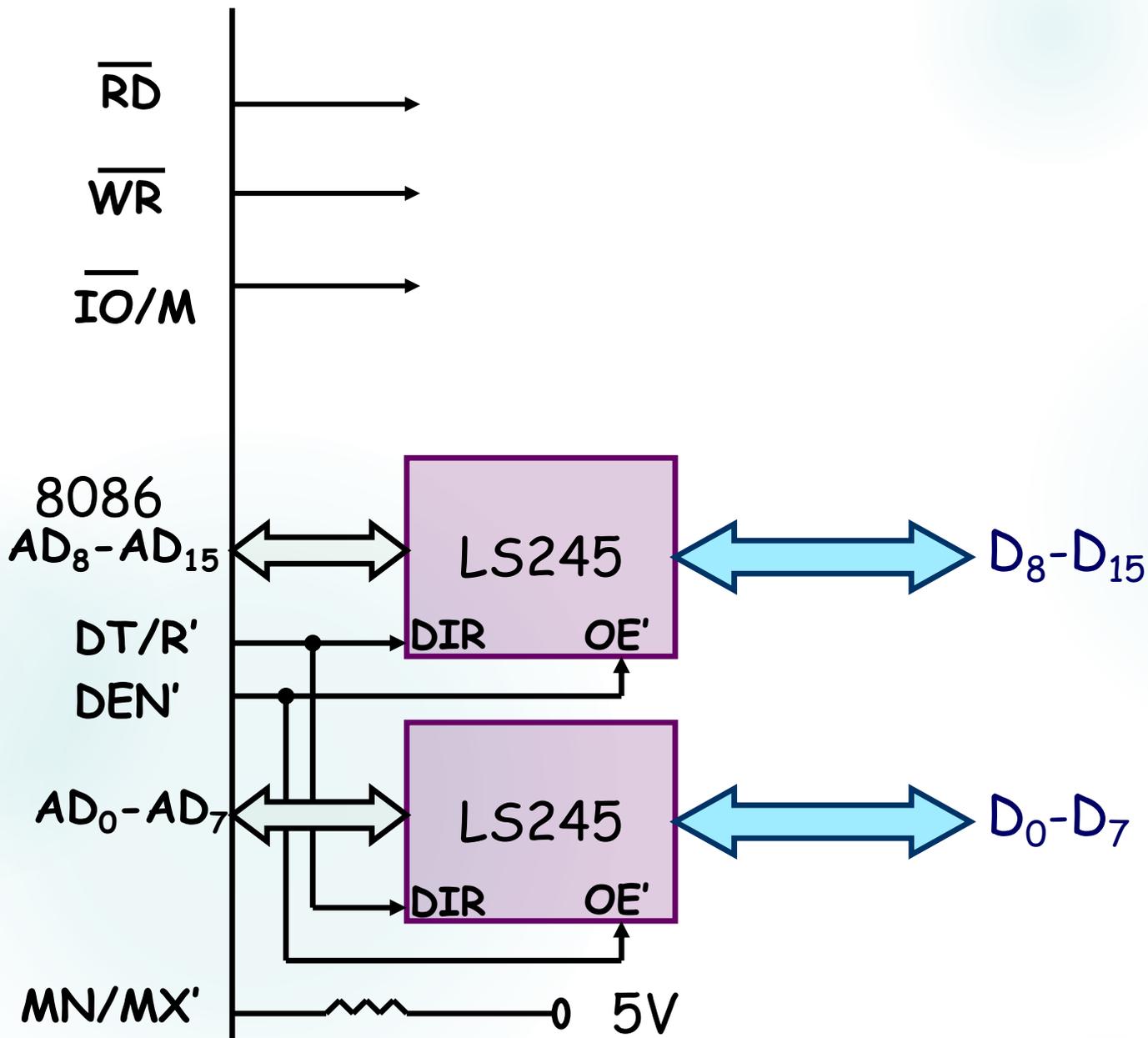


Interface to the processor

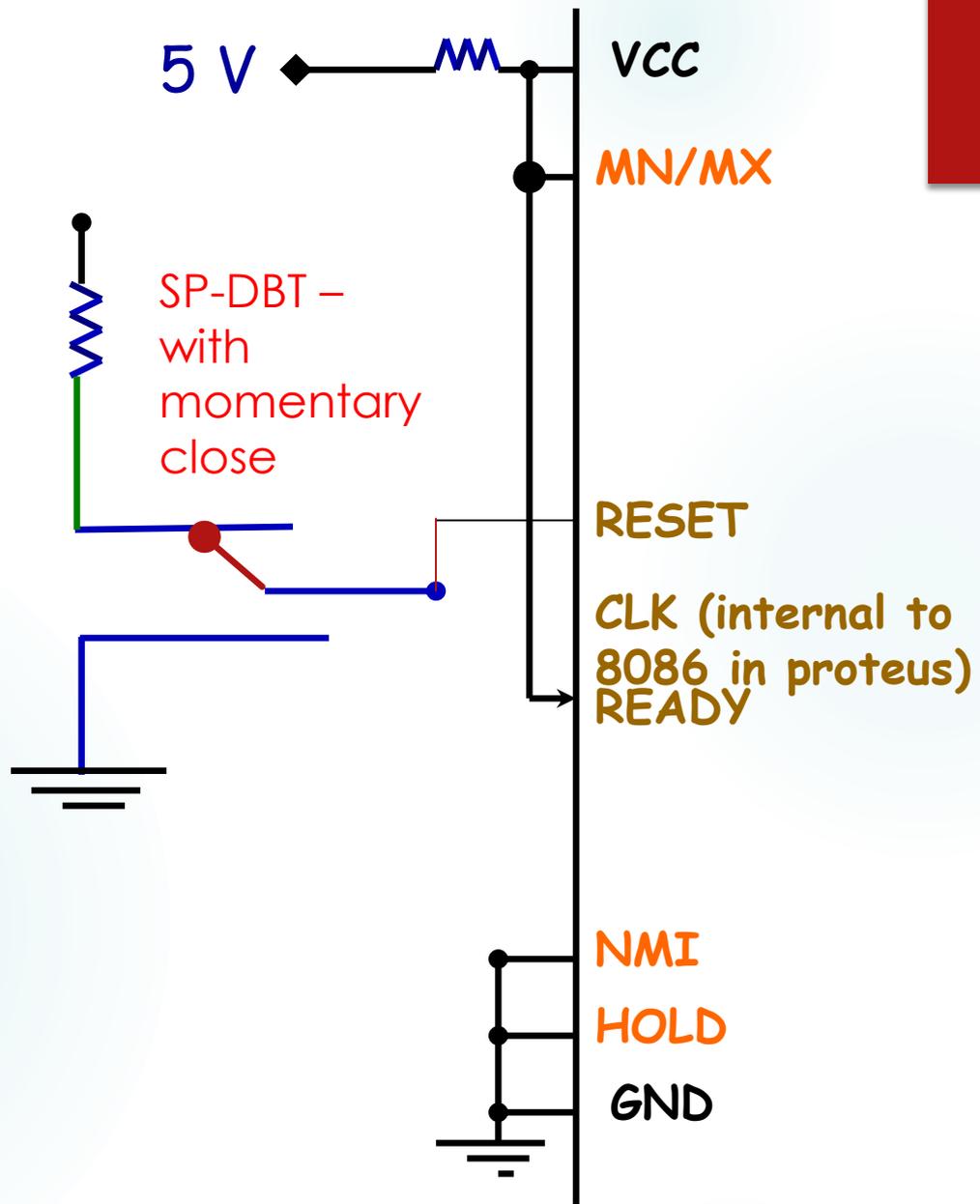




System Bus of 8086 (Address)

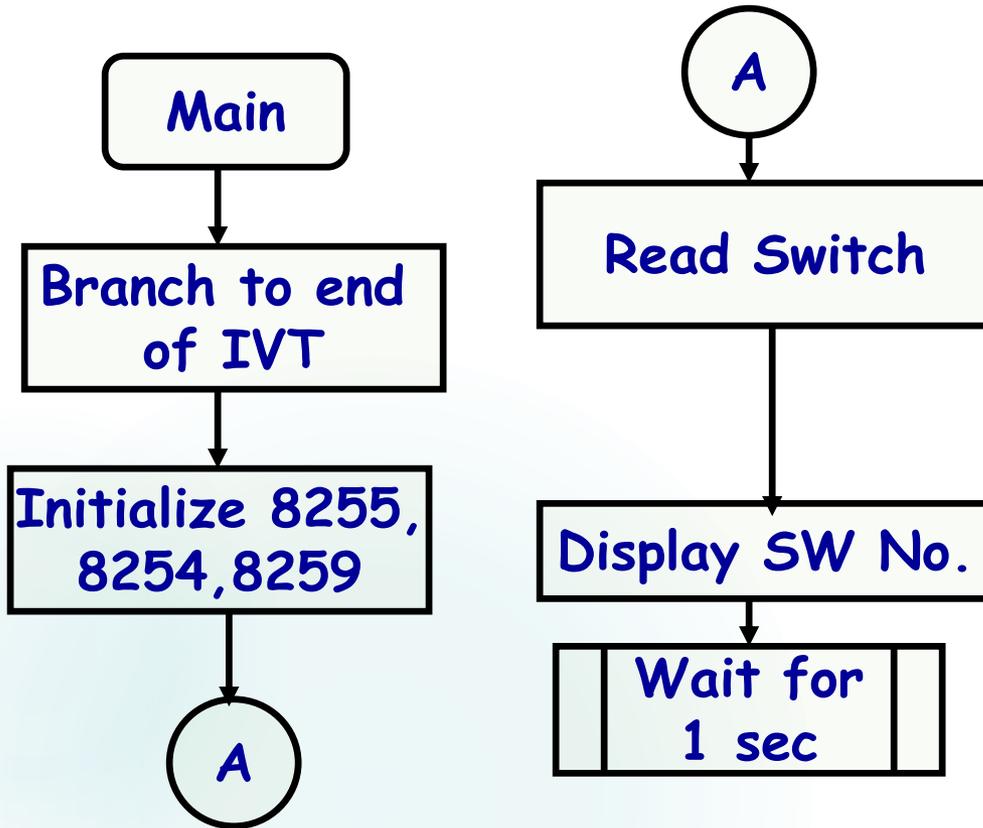


System Bus of 8086(Data + Control)

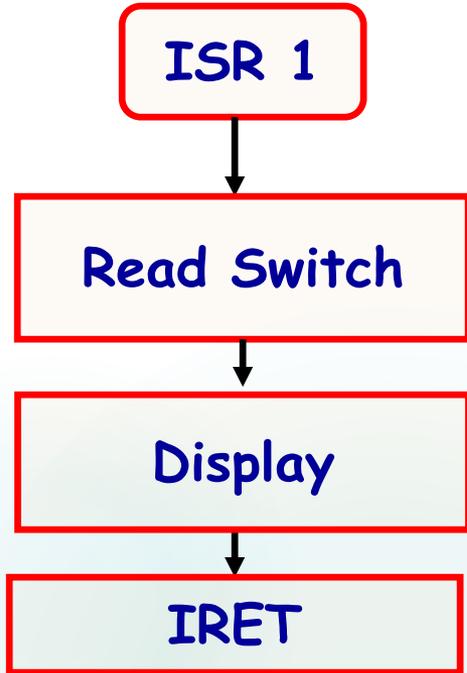


8086 Inputs

Software



Software - ISR



Program

- ▶ Use EMU 8086 for assembling – as it creates the reqd binary file to load to 8086 ROM