CS/ECE/EEE/INSTR F241 – MICROPROCESSOR PROGRAMMING & INTERFACING

MODULE 8: I/O INTERFACING

QUESTIONS

ANUPAMA KR
BITS, PILANI – KK BIRLA GOA CAMPUS

Q1. Distinguish between vectored and non-vectored interrupts with an example.

Q2. Build a hardware circuit that can take in 8 interrupt requests as inputs and generate vector nos. (40H – 47H) for these interrupt requests. What are the main issues with this circuit?

Q3. Using 8255 BSR generate a square waveform of frequency of 2 KHz on PC_0. 8255 base address is $00_{H.}$Write the software segment for programming 8255 to generate the waveform. You can assume that there is a delay routine (delay250) available for generating a delay of 250μs. Show the hardware Interfacing circuit

Q4. Write a sub-routine that would set the odd bits of Port C of 8255 PPI using BSR. Assume that the address of the control register is 06_H.

Q5. There are set of 8 LEDs connected to Port C of 8255- a logic high turns on the LEDs.

- Write a code snippet that will turn on the LEDs connected to the even bits of Port C using BSR mode.
- 8255 is mapped to address 80_H
- Show the complete hardware interfacing circuit from the system bus onwards.

Q6. Design an 8086 based system that will generate a waveform of frequency 500 KHz using 8254 (use 5 MHz Clock) and 10% duty cycle whenever a switch S1 is closed. The output of Switch S1 is logic high when open and logic low when closed.

Chips available:

- 8254 1 no.
- Hex Inverter 1 no.
- LS138 1 no.

Q7. Generate a 5×10^{-6} Hz square wave using 8253/8254.

- Given clock = 2.5 MHz
- Base address = 90H
- Mapping: I/O mapped

Q8. The timer 8254 (operating @ 8MHz) is used to generate interrupt requests at a rate of 500 pulses/sec to NMI Input of processor.

Q9. An 8086 system is used for controlling the speed of the motor. The motor can operate at 5 different speeds (1-5). The speed is changed by changing the duty cycle of a PWM input of frequency 1 KHz to the motor's driver circuit. The PWM duty cycle changes from 30% to 70 % in steps of 10 % for speeds 1 – 5.

The user sets the speed using a series of 5 switches - one for each speed. The user then closes the ON switch to turn on the motor. When the users presses OFF switch the motor has to be closed(only one switch can be closed at any time).Seven segment displays are available on which the duty cycle of the PWM signal is displayed. The displays are always enabled and display the value '00' when the motor is not rotating. The only clock signals available in the system are the 5MHz system clock and 2.5MHz PCLK.

The following interfacing devices are available:

- 8255 01 no. Mapped to address 80H, 82H, 84H, 86H.
- 8253 01 no. Mapped to address 88H, 8AH, 8CH, 8EH.
- A BCD to seven segment decoder. 02 nos.
- Any number of OR gates and inverters for address decoding.

Note: 8253 output cannot be given as input to 8255 and interrupts are not used in this system

Q10. Design an 8086 based system that is used for monitoring the number of objects crossing a particular point in a manufacturing system.

The system works as follows:

- Every minute an interrupt (INT1) is raised to the system.
- When INT1 is raised the system counts the number of objects crossing a point for a period of 1 second.
- The number of objects crossing the point in one second does not exceed 75d.
- The number of objects that have crossed the point must be displayed at the end of 1 second on a pair of 7-segment displays. The display remains the same until the next count.
- There is circuit available at the checkpoint that produces a low pulse (logic0 –TTL) every time an object crosses the point.
- This process of monitoring the point for 1 second is repeated at intervals of 1 minute.
- High accuracy is required for the 1 minute and 1 second delays.
- Show the complete I/O mapping and I/O decoding circuit. (Starting Address: 8255 -00H, 8254s-08H-, 8259- 18H)

Q11. Using 8254 measure the pulse width of a signal. Given clock = 2.5 MHz and Base address = $FF90_H$.

Q12. Design an 8086 based system that will generate a waveform of frequency 500 KHz using 8254 (use 5 MHz Clock) and 10% duty cycle whenever a switch S1 is closed. The output of Switch S1 is logic high when open and logic low when closed.

Chips available:

8254	1 no.
Hex Inverter (Has 6 inverters in a single chip)	1 no.
LS138	1 no.

Show the complete I/O Interfacing and also write the required ALP to initialize 8254 in the appropriate mode. The base address of 8254 is 80_H. The higher address lines $A_8 – A_{19}$ can be ignored. All system bus signals (MEMR', MEMW', IOR', IOW' BHE', A_0- A_{19}, $D_0 – D_{16}$) are available.

Q13. An 8086 system is used for measuring the temperature in a chemical bath.

- The temperature has to be read every 2 seconds- use a timer to accurately generate the time delays.
- The temperature sensor can read temperatures between 0^0C to 250^0C with a resolution of 1^0C
- The sensor output varies between 0- 5 V – with a resolution of approximately 19.6mV/^{0}C
- The temperature should be displayed on 3 seven segment displays.

The only clock signals available in the system are the 5MHz system clock and 2.5MHz PCLK.

Q14. Design a System that receives a burst of ASCII data at speed 4800 baud via 16550

- 8 bytes of data received are stored from a base address of 02000_H
- An DAM Request is raised every time there is 8 bytes of data in the FIFO
- 16550 base address – 40_H
- Use DMAC- base address – 80_H

Q15. What is the application or use of the IORC' and IOWC' signals in a memory mapped I/O system? Do these signals help in accessing the I/O device? Explain briefly.

Q16. Design a System that senses the temperature in a room (there are totally 7 sensors) at regular intervals of 2 minutes and sends it via 16550 – 38,400 baud.

Q17. Write a sub-routine that can be used for transferring data from IO device to memory location using DMAC 8237. The starting address of the DMAC is $A0_H$. The IO Device uses burst transfer of up to 512bytes of data/burst. The starting address of memory location to which the transfer must be done is 02000_H. DMA channel 2 is used by IO Device- IO DREQ is active Low, DACK is active high.

Q17. The first few entries for the Root directory a disk are as given below:

ROOT DIRECTORY

4D 55 50 20 20 20 20 20 – 45 58 45 03 01 00 00 02

02 F3 45 44 3F 48 02 42 – C5 32 07 00 F0 09 00 00

(i) Name of the file is

(ii) The size of the file in KB is

(iii) File Attributes are

(iv) Starting Cluster of the file is

Q18. The timer 8254 (operating @ 8MHz) is used to generate interrupt requests at a rate of 500 pulses/sec at IR2 input of 8259 PIC. The Interrupt is edge triggered and the vector number associated with IR2 is 42_H. There is only one 8259 in the system. Give the required command words for initializing the 8254 and 8259. (Use automatic EOI).

Q19. Write a program to generate a square wave of 1KHz frequency on OUT 1 pin of 8253. Assume CLK1 frequency is 1MHz and address for control register = $0F_H$.

Q20. The first 24 bytes of boot sector of a floppy are given below. All the entries are in hexadecimal. Using these entries answer the following questions. Answers must be in decimal

EB 3C 90 2A 60 59 60 48 - 49 43 0A 00 04 08 02 00

02 40 01 40 1F F0 12 00

A	Number of bytes/sector		E	Total number of sectors/FAT	
B	Number of sectors/cluster		F	Total number of reserved sectors	
C	Number of root directory entries		G	Number of sectors used by a file of size 8448 bytes	
D	Total number of sectors on disk		H	Size of disk in KB	

Q21 The system to be designed is used for Industrial Applications. The Industrial Application has two-level hierarchy. At Level 1 of the hierarchy there is ***Device Control*** and at Level 2 of the hierarchy there is ***Factory Control***. You are supposed to design the system for Device Control.

The specifications of the Device Control system is as follow:

- System is built around the 8086 processor which is working at a frequency of 5 MHz.
- It has 640 KB of memory – of which 256 K is ROM and the rest is RAM – Half of the ROM is mapped to address space starting at 0 00 00_H and half it to address space starting from E 00 00_H The RAM 128 K is mapped from 4 00 00_H and the rest from address 8 00 00_H.

a) Show the complete memory mapping and design the memory interfacing circuit *using only the chips given in table below*. All system bus signals (MEMR', MEMW', IOR', IOW', BHE', A_0- A_{19}, D_0 – D_{15}) are available. Use Absolute Addressing.

Chips Available other than peripheral I/O	Nos.
64 K ROM	4
64 K RAM	6
LS138	2

- In addition the system has *1* 8259, *1* 8255, *1* 16550, *1* 8254s.

b) Show the complete I/O mapping and I/O decoding circuit *using only a single decoder (LS138)*. All system bus signals (MEMR', MEMW', IOR', IOW', BHE', A_0- A_{19}, D_0 – D_{15}) are available. (Starting Address: 8255- $C0_H$, 8254 - $A0_H$, 16550- 80_H, 8259 – 60_H). Use Incremental Addressing.

- The industry manufactures car parts. The ***Device Control System*** is used to calculate number of objects that are produced in 1 second. The number of objects are displayed on four seven-segment displays on the factory floor. The number of objects produced in a second is also sent to the ***Factory Control System*** via a 16550 null modem interface.
- The 7-segment displays are interfaced via 7447 BCD – 7 segment display. There are *four* 7447 available. 7447 is used with Common Anode Display and 4-bit BCD input given will be converted to a 7-segment value.

c) Show all the required hardware connection for 8255 to the System Bus as well as to the display. Displays should not be multiplexed. Write an ALP routine that initializes 8255 and displays "0 0 0 0" on 7-segment display.

- The car parts that are produced leave the manufacturing unit on a conveyer belt- every time a car part enters the conveyer belt – a sensor on the conveyer belt gives a logic high pulse (+5V) output. The pulses have to be counted using 8254 – the maximum number of objects produced in a second will not exceed 5000. The 8254 has to be used for counting the number of objects. The 8254 is also used to generate an interrupt every 1 second. The interrupt has to be high pulse generated every one second by 8254.

d) Show all the required hardware connection for 8254 to the System Bus as well as to the sensor and interrupt. Write an ALP routine that initializes 8254 for counting & Interrupt generation. The only hardware you are allowed to use other than 8254 is a NOT gate.

- The 1 second interrupt generated by 8254 is connected to 8259 IR0. The interrupts are edge triggered and IR0 is mapped to vector number 60_H. Automatic end of Interrupt has to be enabled and only IR0 should be enabled.

e) Show all the required hardware connection for 8259 to the System Bus as well as to IR0. Write an ALP routine that initializes 8259.

- The number of objects produced in a second is also sent to the ***Factory Control System*** via a 16550 null modem interface. The data is sent 8-bits at a time with no parity 1 stop bit at a rate of 19.2 kbps. The 16550 has a separate crystal of 18.432MHz.

f) Show all the required hardware connection for 16550 to the System Bus as well as null modem. Write an ALP routine that initializes 16550.