CS/ECE/EEE/INSTR F241 – MICROPROCESSOR PROGRAMMING & INTERFACING

MODULE 7: MEMORY INTERFACING

QUESTIONS

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Q1. An 8086 based system has the following memory requirements:

- 256K of ROM from 00000_H
- 256K of ROM from $C0000_H$
- 256K of RAM from 60000_H.

Chips available:

64K ROM -8, 64K RAM -4, LS138-2. Design the memory Interfacing circuit.

Q2. For an 80286 processor that has 16 MB of memory of which 4M is ROM and the rest is RAM. Half of the ROM - mapped to address space starting at 00 00 00_H Half to address space starting from E0 00 00_H. The RAM is mapped continuously from address 20 00 00_H. Design the memory Interfacing circuit.

Q3. For an 8086 based system with the following memory requirements:

SRAM: 16KB from 02000_H
ROM: 16 KB from 09000_H

The following chips are available

- SRAM- 2K x 8bit ROM- 2K x 8bit
- 74138 decoders (4 numbers)

Using these decoders and minimum number of logic gates draw the memory interfacing diagram

Q4. An 8086 system has the following memory requirements:

384K of ROM from 00000_H

384K of ROM from $A0000_H$

256K of RAM from 60000_H

The following chips are available

32K ROM -24

32K RAM - 8

LS138 -4

Design the memory Interfacing circuit.

Q5. Design an 80286 based system that has the following memory requirements:

1 M of ROM from 000000_H
1 M of ROM from 800000_H
1 M of ROM from $F00000_H$
7 M of RAM from 100000_H
3 M of RAM from 900000_H

Chips available:

512K ROM chip	6 nos.
512K RAM chip	20 nos.
LS138	4 nos.

Show the complete memory mapping and design the memory decoding circuit ***using only the chips given***. All system bus signals (MEMR', MEMW', IOR', IOW' BHE', A_0- A_{23}, D_0 – D_{16}) are available. Show the memory interfacing circuit. **Use absolute addressing.**

Q6. A **System** is built around the 8086 processor which is working at a frequency of 5 MHz. It has 640 KB of memory – of which 256 K is ROM and the rest is RAM – Half of the ROM is mapped to address space starting at 0 00 00_H and half it to address space starting from E 00 00_H The RAM 128 K is mapped from 4 00 00_H and the rest from address 8 00 00_H.

Show the complete memory mapping and design the memory interfacing circuit *using only the chips given in table below*. All system bus signals (MEMR', MEMW', IOR', IOW', BHE', A_0- A_{19}, D_0 – D_{15}) are available. Use Absolute Addressing.

Chips Available	Nos.
64 K ROM	4
64 K RAM	6
LS138	2

Q7. **80286-based system has the following memory requirements**

576KB of memory

128KB	ROM
rest	RAM

The mapping is as follows

64 K ROM	000000_H
64 K ROM	$0F0000_H$
RAM	040000_H

System is expandable in nature.

Chips available:

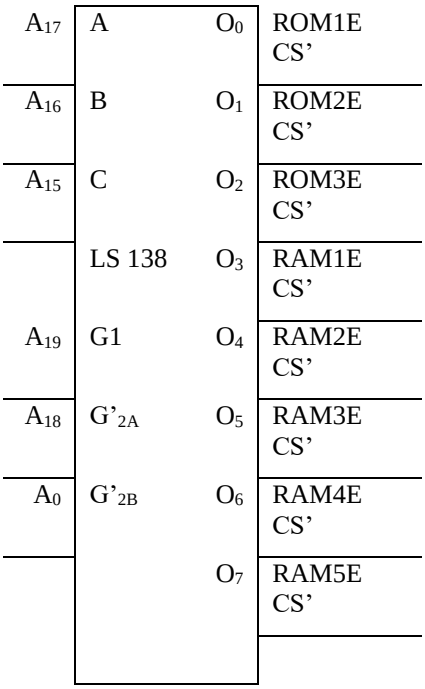
27256	4 nos.
61256	14 nos.
Inverter	1
LS138	4 nos
4-input OR gates	1

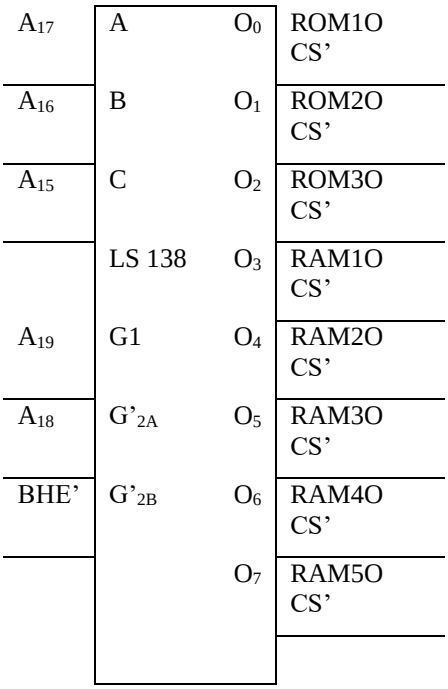
Design the memory interfacing circuit.

Q8. For an 80386 system with the following memory requirements - 1 M SRAM – 04 00 00 00_H

The SRAM chip available is MS621000 128 K x 8. The memory interfacing has to be done using GAL22V10C. (Refer to corresponding video for details of GAL22V10C)

1. **Q9.** The decoding logic **(using absolute addressing)** for an 8086 processor is shown below. This is the only decoding circuit in the computing system and the rest of the address lines are used with the memory chips. (Pin out of this decoder is same as the one given in Lecture 1 of Module 7)





Answer the following questions

How much memory does the system have? How much of this memory is RAM? What is the size of the RAM and ROM Chips used? What is the memory map?

Memory Chips	**Address [Starting Address-Ending Address]**	**Memory Chips**	**Address [Starting Address-Ending Address]**
ROM1		**RAM2**	
ROM2		**RAM3**	
ROM3		**RAM4**	
RAM1		**RAM5**	