CS/ECE/EEE/INSTR F241 – MICROPROCESSOR PROGRAMMING & INTERFACING

MODULE 5: PINOUT OF 8086

QUESTIONS

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Q1. What are the signals available on the system bus?

Q2. Can ALE inverted be used instead of DEN for enabling the transceivers?

Q3. What signals of 8088 are different from 8086?

Q4. Give the machine cycles that have to be carried out for the following instructions for 8086

Call AX

RET (near)

ADC AX,BX

ADD AX,[BX]

DEC WORD PTR [SI]

MOV CX,DX

MOV CL,DAT1

ROL BYTE PTR [2000], CX (CX has a count of 7)

Call 8000H

Q5. For the following Instructions what will be the machine cycles executed by 8086. (Machine cycles in proper order)

ADD [BX+SI+1000H] , CX

XCHG AX,[BX]

NOP

CMP [SI],AX

Q6. If a processor is working at 5 MHz and the memory access time is 750ns. The number of wait states required will be _____ , considering an address set-up time of 110ns, data set-up time of 40ns with a latching and buffer delays of 30ns.

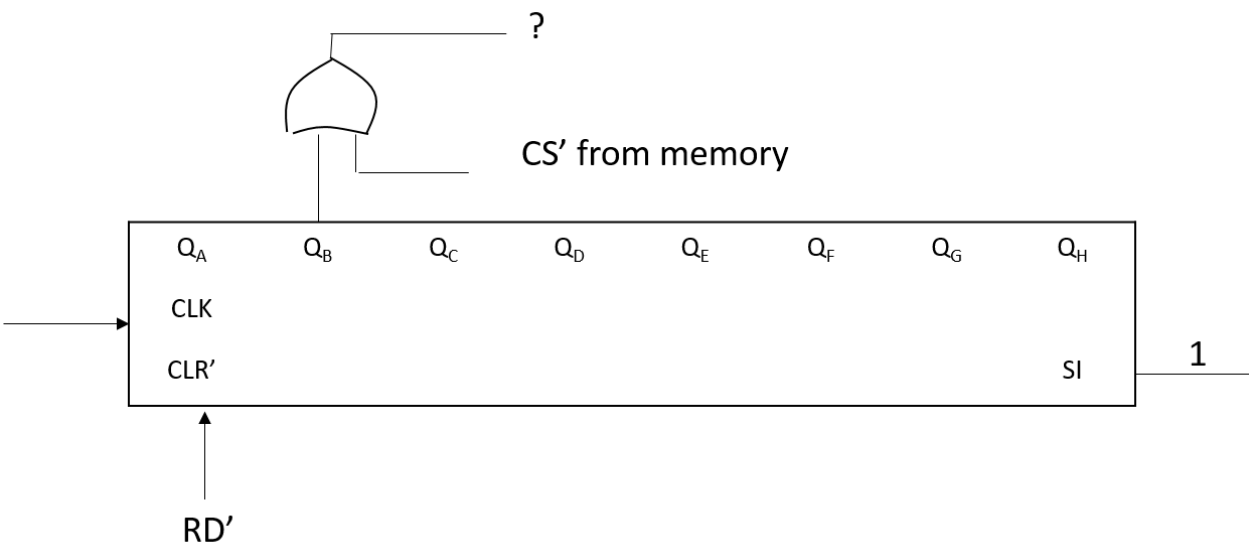
Q7. If an 8086 processor is working at 5 MHz – how much time does 1 MEMR cycle take

If there no wait states

If there is 1 wait state

Q8. If the microprocessor is working at 5 MHz and memory access time is 500 ns how many wait sates will be required?

Q9. For the ckt below how many ready states will be generated? When? Where should this signal be connected?



Q10. Is it possible that during any active bus cycle of 8086 both RD'and WR'are high? Elucidate.

Q11. If NMI, INTR and HOLD all become active at the beginning of executing the instruction MOV BX, [2010H]. Which input to the processor will be serviced first and why?

Q12. What is LOCK'? Describe its function using an example?