CS/ECE/EEE/INSTR F241 – MICROPROCESSOR PROGRAMMING & INTERFACING

MODULE 10: ADVANCED TOPICS

QUESTIONS

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Q1. Modify the time slice scheduling program to have non-pre-emptive priority, FAIR Scheduling.

Q2. The table below shows the current execution order of threads in various time slots in a multi-threading system. The threads which are completed in the current execution time are shown by time slots that are shaded.

Fill in the threads that will be executed in timeslots 11 -14 – assuming that no new threads are available for execution

THREAD	TH1	TH2	TH3	TH4	TH5	TH6	TH7	TH8	TH9	TH10
TIME SLOT										
THREAD	TH2	TH3	TH6	TH7						
TIME SLOT										

Q3. If the DPL of a call gate is 11 and the RPL of the selector within the Call gate is 01 – what should the minimum CPL and RPL of the selector if an application task wants to use the call gate?

Q4. If the current **CPL** is 10 and **RPL** is 01 the only tasks that can be accessed without a gate are the ones that have a DPL of _____

Q5. The OS of an 80286 processor supports non-preemptive priority scheduling. There are 5 threads that have to be scheduled. The tasks and priority are shown in the table below.

Thread	TH1	TH2	TH3	TH4	TH5
Priority	1	4	2	5	3

Give the order of the threads scheduled in the 1st five timeslots.

Q6. Assume that the system has a two-level cache:

- The level-1 cache has a hit rate of 90% and the level-2 cache has a hit rate of 97%.
- The level 1 cache access time is 4 ns, the level 2 cache access time is 15ns and access time of main memory is 80 ns.
- What is the average memory access time?

Q7. If we want an average memory access time of 6.5ns, Cache access time is 5 ns. Main memory access is 80 ns. What cache hit rate must we achieve?

Q8. The following data is present in memory of size 16 locations

0000	F8
0001	56
0010	3A
0011	79
0100	67
0101	8D
0110	9B
0111	78
1000	91

1001	AD
1010	BC
1011	78
1100	96
1101	70
1110	00
1111	FF

If the data is read by the processor in the following order from the addresses

- 0000
- 0001
- 0100
- 1000

Show the contents of the cache for direct-mapped; four line cache with each read operation. Repeat the problem if the cache for 2 way set associative, two line cache after every read operation.

Q9. There is only a single cache in processor based system and the cache access time is 10ns with a hit rate of 92%. The main memory access time is 25ns what is the average memory access time?

Q10. What are the three types of cache misses?

Q11. If the hit rate of the L1 cache in the system is 90%. The L1 cache access time is 10 ns and the memory access time is 50 ns. What is average memory access time?

Q12. What is the type of miss that you can reduce by changing the cache organization from direct mapped to set associative?

Q13. What is the main difference between 80486 SX and 80486 DX ?

Q14. What are the main differences between the architecture of 80386 and 80486?